

ELEX 3120/3321: Electric Circuits 2

LAB 2 - Comparators

|  |  |  |
| --- | --- | --- |
| Student Name: Enze Xu | Student Number:A01336393 | Set:B |

Table of Contents

[1 Introduction 4](#_Toc178502659)

[2 Pre-Lab 4](#_Toc178502660)

[2.1 MATLAB Code to Simulate a VTD DAQ System 4](#_Toc178502661)

[3 Non-Inverting Comparator 5](#_Toc178502662)

[3.1 Design a non-inverting comparator with Vref = 3 V 5](#_Toc178502663)

[3.2 Simulate the Design 6](#_Toc178502664)

[3.3 DC Test of Design 6](#_Toc178502665)

[3.4 VTD Test of Design 7](#_Toc178502666)

[4 Inverting Comparator 7](#_Toc178502667)

[4.1 Design an inverting comparator with Vref = -3 V 7](#_Toc178502668)

[4.2 Simulate the Design 8](#_Toc178502669)

[4.3 DC Test of Design 8](#_Toc178502670)

[4.4 VTD Test of Design 9](#_Toc178502671)

[5 Non-Inverting Comparator with Hysteresis 9](#_Toc178502672)

[5.1 Design a comparator with VUT = 5 V and VLT = 3 V 9](#_Toc178502673)

[5.2 Simulate the Design 10](#_Toc178502674)

[5.3 DC Test of Design 10](#_Toc178502675)

[5.4 VTD Test of Design 11](#_Toc178502676)

[6 MATLAB Code for VTD Plots 11](#_Toc178502677)

[7 Conclusions 12](#_Toc178502678)

Table of Figures

[Figure 1 - MATLAB VTD SIMULATION PLOT 5](#_Toc178500757)

[Figure 2 - LTspice Schematic of Non - Inverting Comparator 5](#_Toc178500758)

[Figure 3 - VTD Simulation of Non - Inverting Comparator 6](#_Toc178500759)

[Figure 4 - VTD Test of Non - Inverting Comparator 7](#_Toc178500760)

[Figure 5 - LTSpice Schematic of Inverting Comparator 7](#_Toc178500761)

[Figure 6 - VTD Simulation of Inverting Comparator 8](#_Toc178500762)

[Figure 7 - VTD Test of Inverting Comparator 9](#_Toc178500763)

[Figure 8 - LTSpice Schematic of Non - Inverting Hysteresis Circuit 10](#_Toc178500764)

[Figure 9 - VTD Simulation of Non - Inverting Hysteresis Circuit 10](#_Toc178500765)

[Figure 10 - VTD Test of Non - Inverting Hysteresis Circuit 11](#_Toc178500766)

Table of Tables

[Table 1 - DC Test Output Voltage of Non - Inverting Comparator 6](#_Toc178500633)

[Table 2 - DC Test Output Voltage of Inverting Comparator 8](#_Toc178500634)

[Table 3 - DC Test Saturation And Threshold Voltage of Non - Inverting Hysteresis Circuit 10](#_Toc178500635)

# Introduction

In this lab, you will develop and experiment with a variety of comparator circuits, including non-inverting, inverting, and hysteresis circuits. Become familiar with MATLAB and the MATLAB programming language syntax. Become familiar with the MATLAB data acquisition (DAQ) module, primarily on using MATLAB and data acquisition (DAQ) to generate Voltage Transfer Diagrams.

# Pre-Lab

## MATLAB Code to Simulate a VTD DAQ System

close all; % Close all figures

% Define the range of Vin from -10V to 10V and back to -10V in 0.1V steps

Vin = [-10:0.1:10, 9.9:-0.1:-10];

% Initialize Vout array with zeros

Vout = zeros(size(Vin));

% FOR loop to set Vout = -10 when Vin < 5, Vout = 10 otherwise

for i = 1:length(Vin)

if Vin(i) < 5

Vout(i) = -10;

else

Vout(i) = 10;

end

end

% Generate the VTD plot (Vout vs Vin)

figure;

plot(Vin, Vout, 'LineWidth', 2);

grid on;

% Label the axes

xlabel('Vin','FontSize',12);

ylabel('Vout','FontSize',12);

% Title for the plot

title('Vout vs Vin','FontSize', 14);

A graph with a line drawn on it

Description automatically generated

Vref = 5 V

-Vsat = -10 V

+Vsat = 10 V

Figure 1 - MATLAB VTD SIMULATION PLOT

# Non-Inverting Comparator

## Design a non-inverting comparator with Vref = 3 V



Figure 2 - LTspice Schematic of Non - Inverting Comparator

## Simulate the Design

A graph with green lines

Description automatically generated

V( Vin)

Vref = 3 V

-Vsat = -10 V

+Vsat = 10 V

Figure 3 - VTD Simulation of Non - Inverting Comparator

## DC Test of Design

|  |  |  |
| --- | --- | --- |
| Non-Inverting | Predicted | Measured |
| Vin (V) | Vout (V) | Vout (V) |
| 1 | -10 | -8.75 |
| 5 | 10 | 9.97 |

Table 1 - DC Test Output Voltage of Non - Inverting Comparator

Measured Vref  = 2.97 [V]

## VTD Test of Design

A diagram with a line

Description automatically generated

+Vsat = 9.97 V

-Vsat = -8.75 V

Vref = 2.97 V

Figure 4 - VTD Test of Non - Inverting Comparator

# Inverting Comparator

## Design an inverting comparator with Vref = -3 V



Figure 5 - LTSpice Schematic of Inverting Comparator

## Simulate the Design

A graph with green lines

Description automatically generated

V( Vin)

Vref = -3 V

+Vsat = 10 V

-Vsat = -10 V

Figure 6 - VTD Simulation of Inverting Comparator

## DC Test of Design

|  |  |  |
| --- | --- | --- |
| Inverting | Predicted | Measured |
| Vin (V) | Vout (V) | Vout (V) |
| -5 | 10 | 9.97 |
| 2 | -10 | -8.75 |

Table 2 - DC Test Output Voltage of Inverting Comparator

Measured Vref  = -3.07 [V]

## VTD Test of Design

A diagram with a line graph

Description automatically generated

Vref = -3.07 V

-Vsat = -8.75 V

+Vsat = 9.97 V

Figure 7 - VTD Test of Inverting Comparator

# Non-Inverting Comparator with Hysteresis

## Design a comparator with VUT = 5 V and VLT = 3 V



Figure 8 - LTSpice Schematic of Non - Inverting Hysteresis Circuit

## Simulate the Design

A graph with a blue line

Description automatically generated

+Vsat = 10 V

-Vsat = -10 V

V(UT) = 5 V

V(LT) = 3 V

Figure 9 - VTD Simulation of Non - Inverting Hysteresis Circuit

## DC Test of Design

|  |  |  |
| --- | --- | --- |
| Hysteresis | Predicted | Measured |
| Vsat- [V] | -10 | -8.76 |
| Vsat+ [V] | 10 | 9.65 |
| VLT [V] | 3 | 3.1 |
| VHT [V] | 5 | 4.8 |

Table 3 - DC Test Saturation And Threshold Voltage of Non - Inverting Hysteresis Circuit

## VTD Test of Design

A diagram with a line graph

Description automatically generated

+Vsat = 9.65 V

V(LT) = 3.1 V

V(UT) = 4.8 V

-Vsat = -8.76 V

Figure 10 - VTD Test of Non - Inverting Hysteresis Circuit

# MATLAB Code for VTD Plots

% Setup DAQ session

s = daq.createSession('ni');

addAnalogOutputChannel(s, 'myDAQ1', 0, 'Voltage'); % output for voltage

addAnalogInputChannel(s, 'myDAQ1', 0, 'Voltage'); % Input for reading output

% Comparator with Hysteresis VTD Simulation in MATLAB

Vin\_values = -10:0.1:10; % Sweep Vin from -10V to +10V

Vin\_values2 = 10:-0.1:-10; % Sweep Vin from +10V to -10V

Vout\_values\_hysteresis = zeros(size(Vin\_values)); % Initialize Vout

Vout\_values\_hysteresis2 = zeros(size(Vin\_values));

for i = 1:length(Vin\_values)

% Output the current Vin to DAQ

outputSingleScan(s, Vin\_values(i));

pause(0.1); % Wait for system to stabilize

% Read comparator output and store it

Vout\_values\_hysteresis(i) = inputSingleScan(s);

end

for i = 1:length(Vin\_values2)

% Output the current Vin to DAQ

outputSingleScan(s, Vin\_values2(i));

pause(0.1); % Wait for system to stabilize

% Read comparator output and store it

Vout\_values\_hysteresis2(i) = inputSingleScan(s);

end

% Create the VTD plot with hysteresis

figure;

plot(Vin\_values, Vout\_values\_hysteresis, '-');

hold on;

plot(Vin\_values2, Vout\_values\_hysteresis2, '-');

title('Voltage Transfer Diagram (VTD) with Hysteresis');

xlabel('Vin [V]');

ylabel('Vout [V]');

grid on;

# Conclusions

In this lab, we successfully built three comparator circuits referred to the LTSpice diagrams, performed DMM measurement on the output side under required voltage input levels. A sweep voltage source programmed in MATLAB was used to provide a varying VIn , incrementing from -10 to 10 V, and back to -10 V in 0.1 V step. Finally, a VTD test diagram helped to verify the simulations and predictions.